

SKW Associates, Inc.

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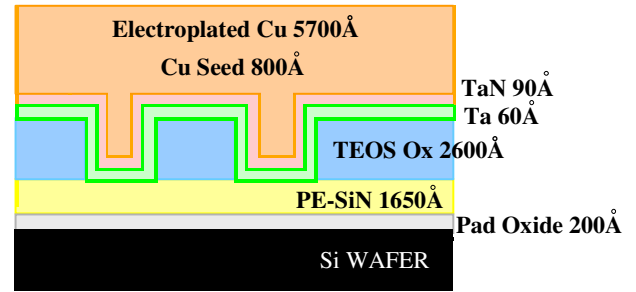
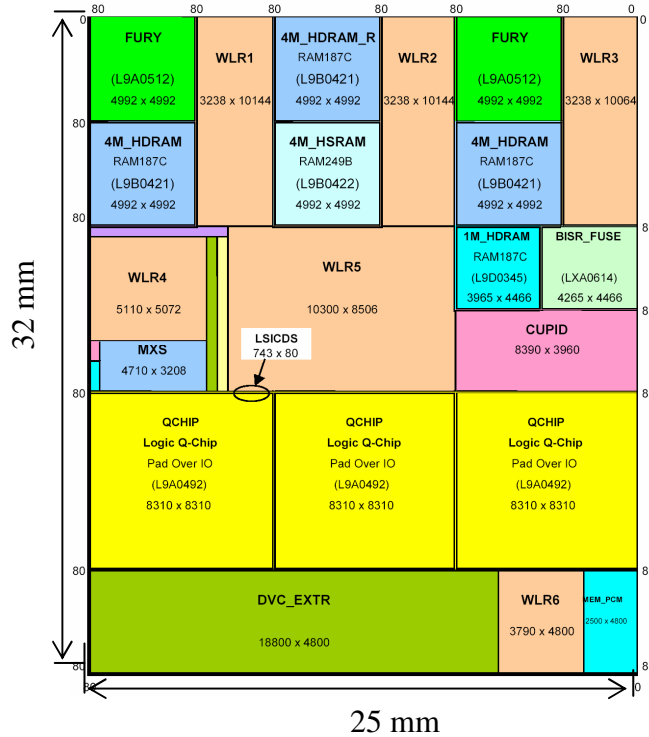
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SKW 6-6 Cu/TEOS V1.0

Wafer Specifications

DATE: August 3, 2006



Cross Sectional View

SKW 6-6 Cu/TEOS Mask Floor Plan

PARAMETER	NOMINAL	TOLERANCE
Patterning		
Center Die X Location	-14.01 mm	+/- 100 μm
Center Die Y Location	-12.41 mm	+/- 100 μm
Die Size: X	25 mm	+/- 10 μm
Die Size: Y	32 mm	+/- 10 μm
Die Stepping (X /Y)	244 / 210 μm	+/- 10%

Wafers must be patterned all the way to the edges of the wafer, i.e. no area anywhere on the wafer unpatterned. (Under certain stepper operating conditions, 2 mm edge edge exclusion is allowed.)

PARAMETER	NOMINAL	TOLERANCE
Line CD Variation (measured on 2 μm structure)		
Lot-to-Lot	2 μm	+/- 10 nm
Within-Lot (Wafer-to-Wafer)		+/- 10 nm
Within-Wafer		+/- 10 nm
Within-Die (measured on 9 trenches)		+/- 10 nm
Pad Oxide thickness		
Lot-to-Lot	200 \AA	+/- 5 %
Within-Lot (Wafer-to-Wafer)		+/- 5 %
Within-Wafer		+/- 3 %
Within-Die		+/- 3 %
SiN film thickness		
Lot-to-Lot	1650 \AA	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
TEOS Oxide film thickness		
Lot-to-Lot	2600 \AA	+/- 8 %
Within-Lot (Wafer-to-Wafer)		+/- 8 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
PVD Ta film thickness		
Lot-to-Lot	60 \AA	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %

PARAMETER	NOMINAL	TOLERANCE
PVD TaN film thickness		
Lot-to-Lot	90 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
PVD Cu film thickness		
Lot-to-Lot	800 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
ECD Cu film thickness		
Lot-to-Lot	5700 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %