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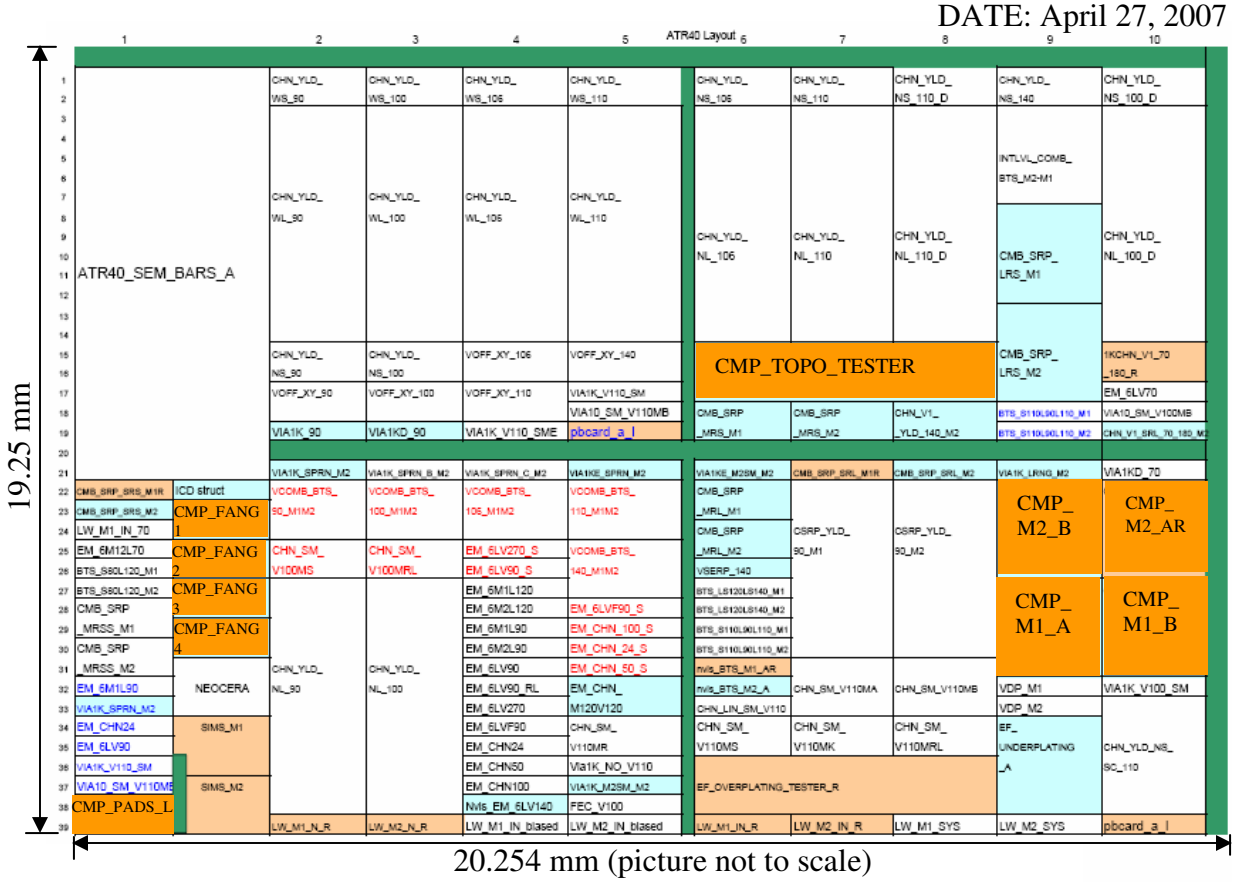
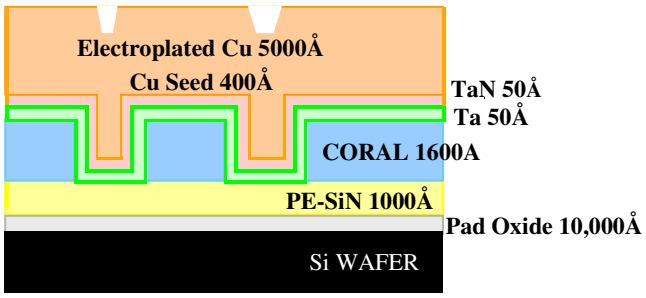
ATR-40 M1 Cu/CORAL (65 nm Tech Node) Wafer Specifications

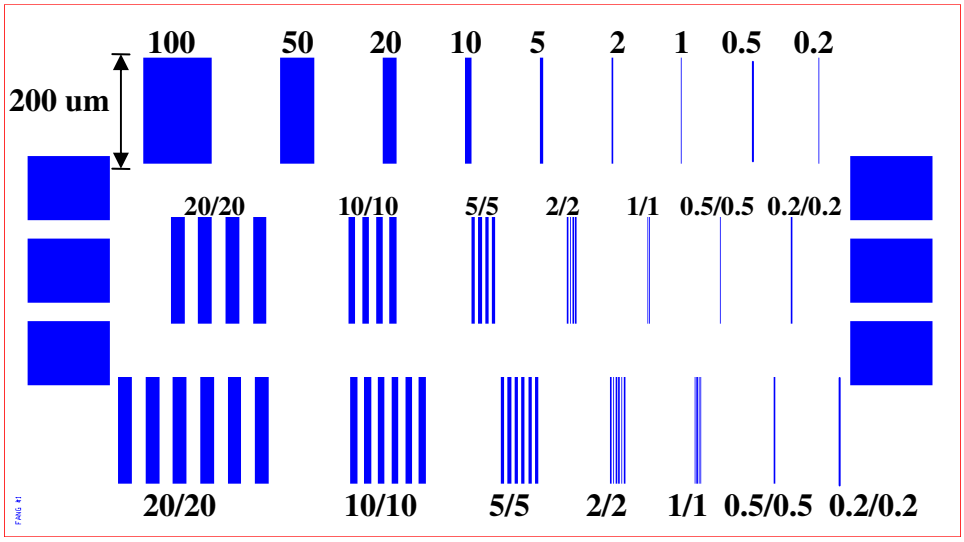
DATE: April 27, 2007



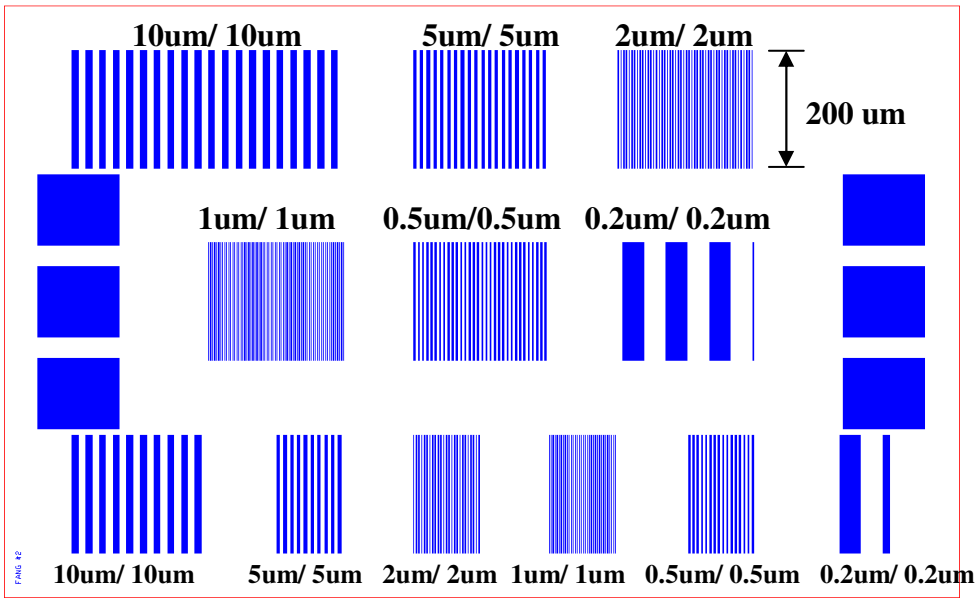
ATR-40 Cu/CORAL Mask Floor Plan
(CMP test structures highlighted in orange)



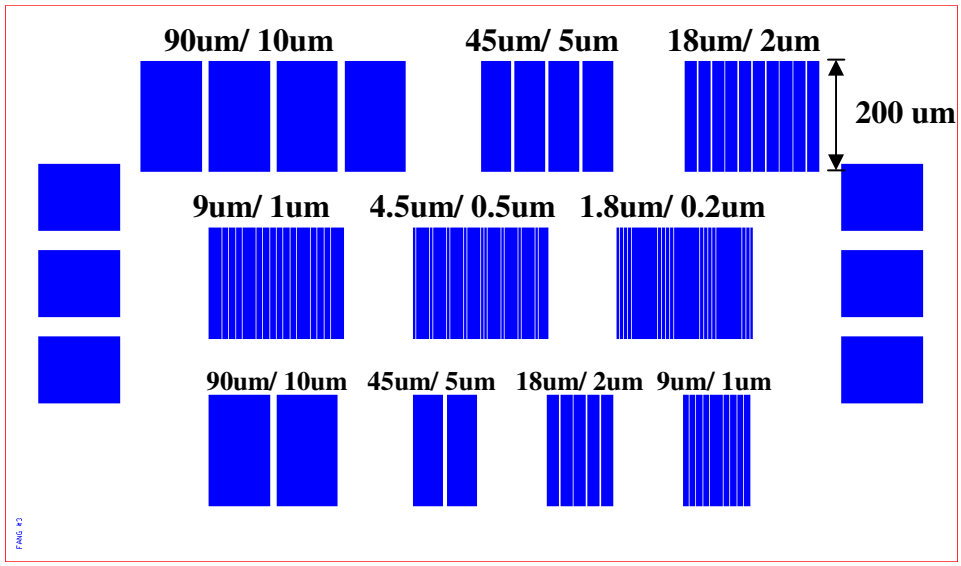
Cross Sectional View



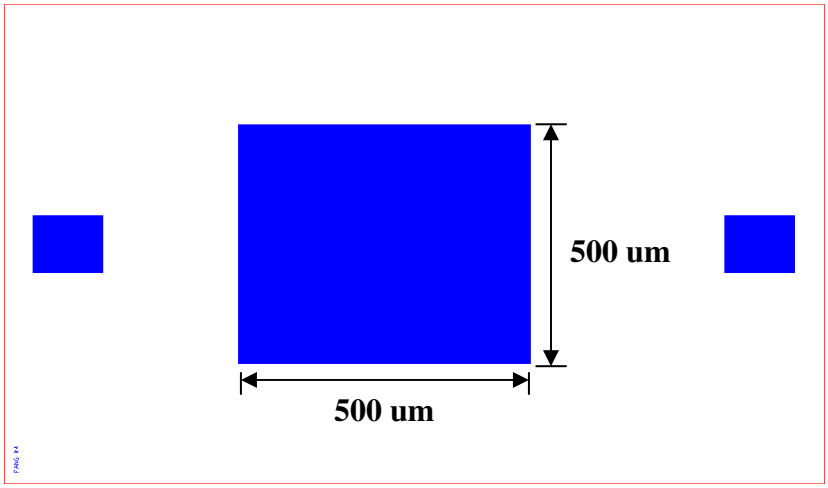
CMP_FANG1 Test Structure



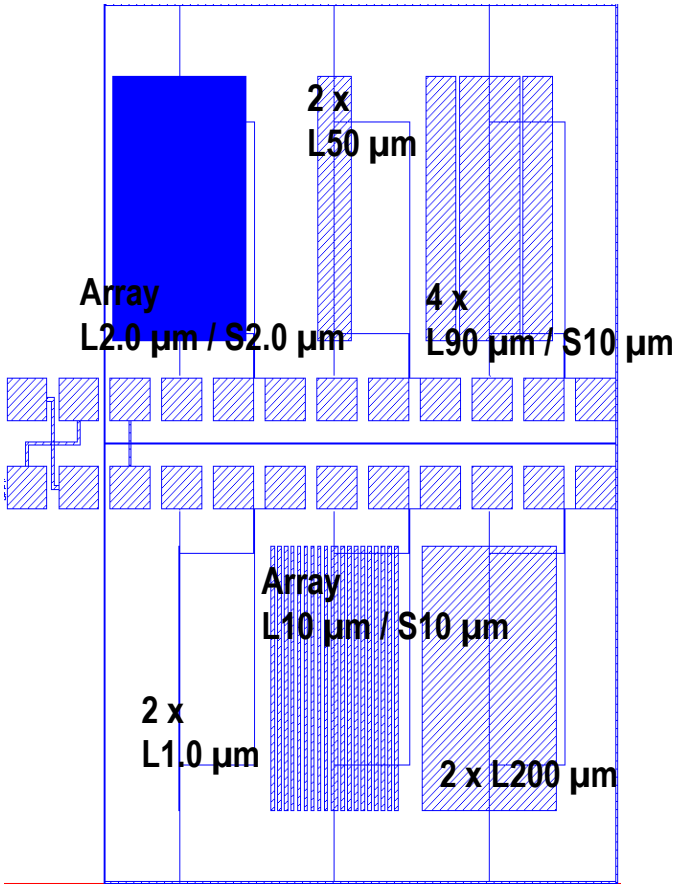
CMP_FANG2 Test Structure



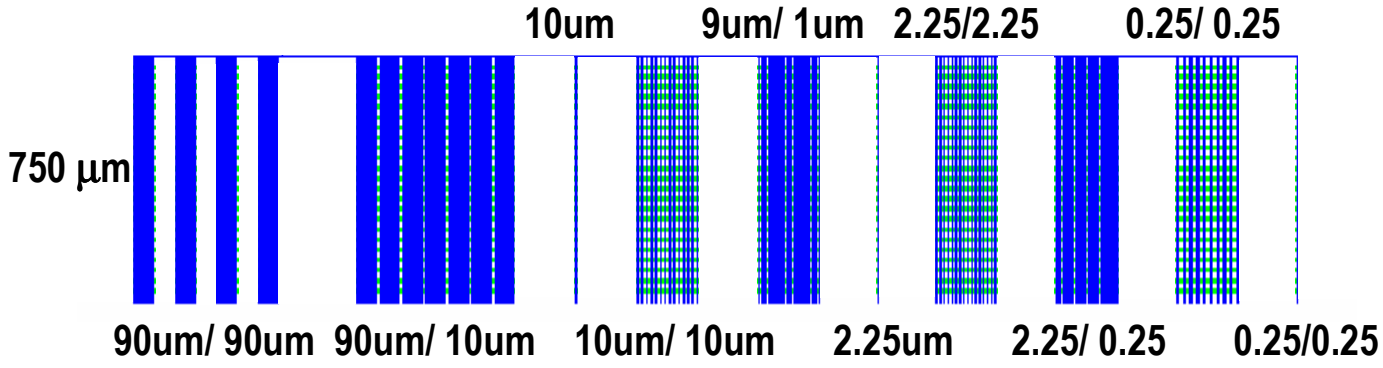
CMP_FANG3 Test Structure



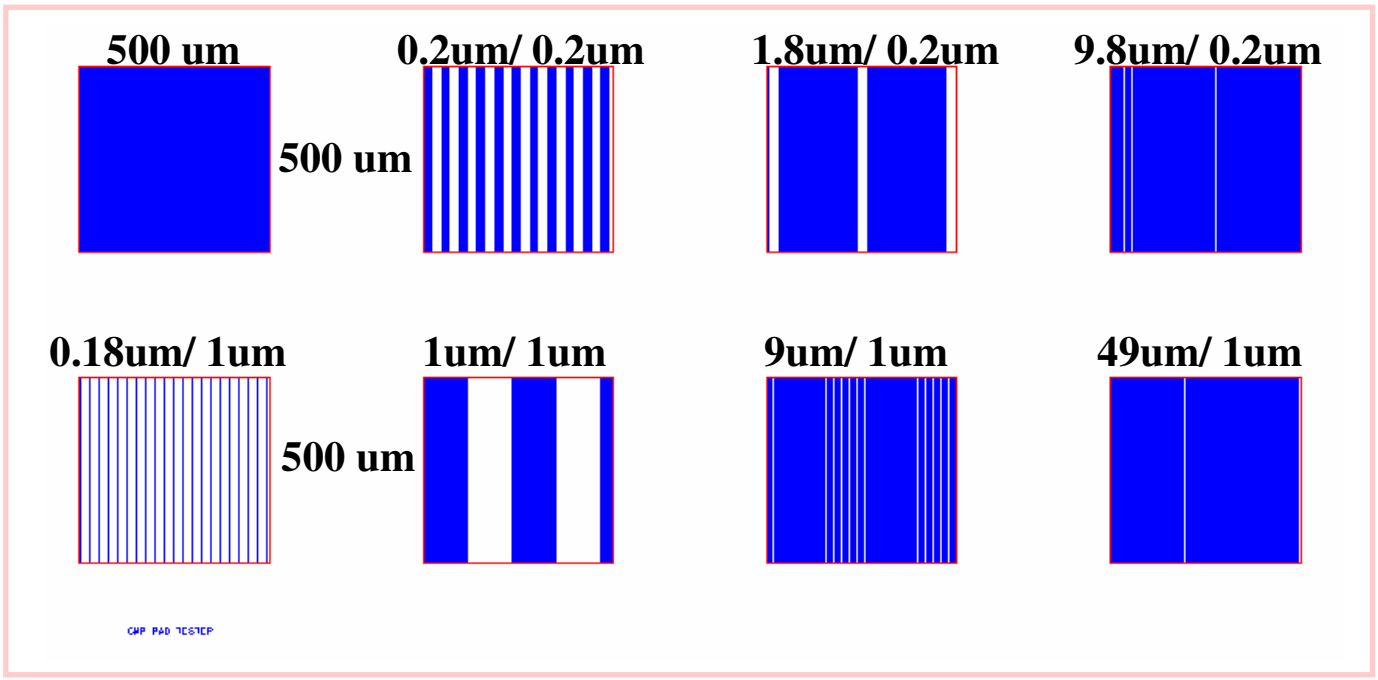
CMP_FANG4 Test Structure



CMP_M1_A E-Test Structure



CMP_TOPO_TESTER Test Structure



CMP_PAD Test Structure (M1 Level)

PARAMETER	NOMINAL	TOLERANCE
Patterning		
Center Die X Location	-1.150 mm	+/- 100 µm
Center Die Y Location	-1.000 mm	+/- 100 µm
Die Size: X	20.130 mm	+/- 10 µm
Die Size: Y	19.113 mm	+/- 10 µm
Die Stepping (X /Y)	136 / 122 µm	+/- 10%
Wafers must be patterned all the way to the edges of the wafer, i.e. no area anywhere on the wafer unpatterned. (Under certain stepper operating conditions, 2 mm edge edge exclusion is allowed.)		
Line CD Variation (measured on 2 µm structure)		
Lot-to-Lot	2 µm	+/- 10 nm
Within-Lot (Wafer-to-Wafer)		+/- 10 nm
Within-Wafer		+/- 10 nm
Within-Die (measured on 9 trenches)		+/- 10 nm
Pad Oxide thickness		
Lot-to-Lot	10,000 Å	+/- 5 %
Within-Lot (Wafer-to-Wafer)		+/- 5 %
Within-Wafer		+/- 3 %
Within-Die		+/- 3 %
SiN film thickness		
Lot-to-Lot	1000 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
CORAL film thickness		
Lot-to-Lot	1600 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %

PARAMETER	NOMINAL	TOLERANCE
PVD Ta film thickness		
Lot-to-Lot	50 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
PVD TaN film thickness		
Lot-to-Lot	50 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
PVD Cu film thickness		
Lot-to-Lot	400 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
ECD Cu film thickness		
Lot-to-Lot	5000 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %