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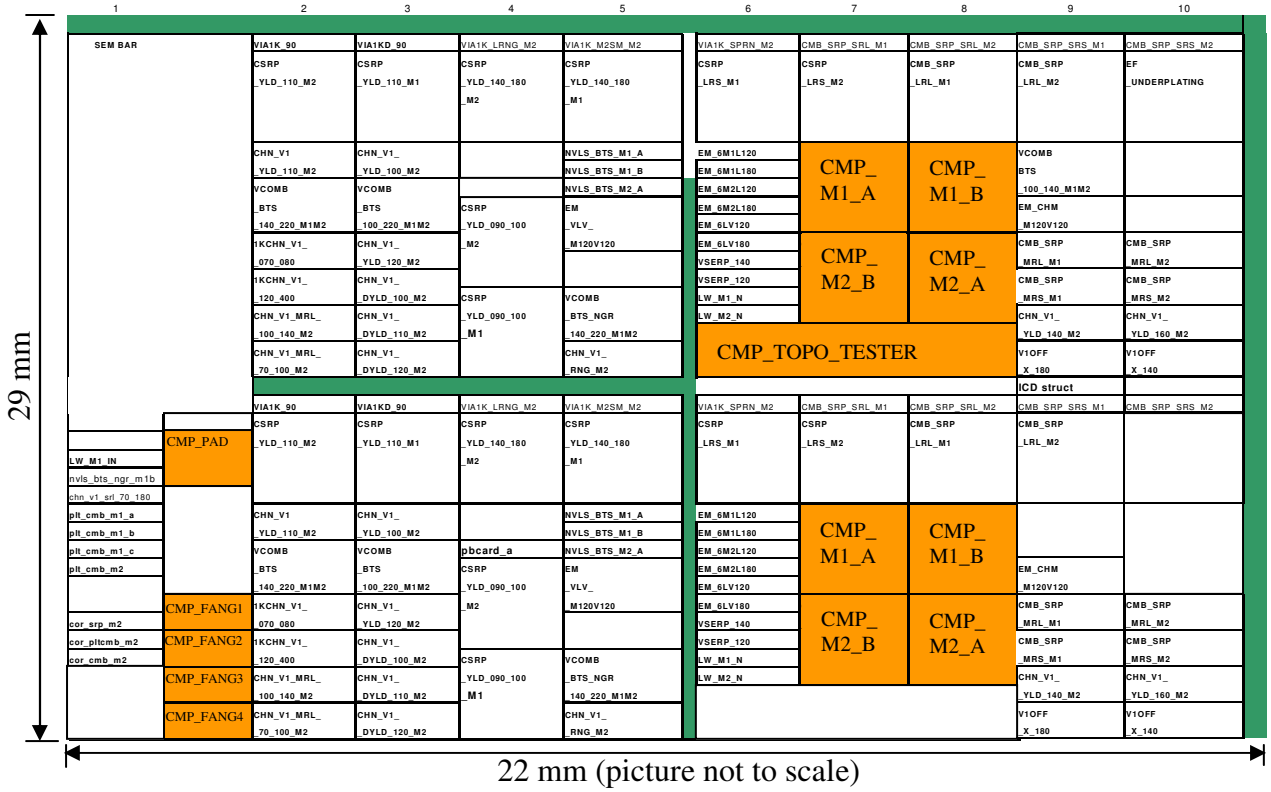
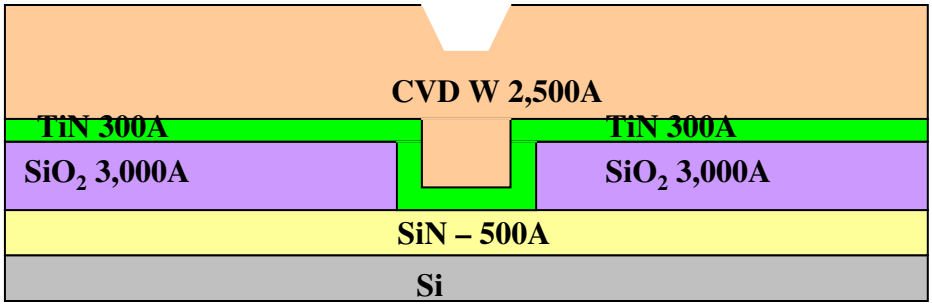
SKW5-ATR-35P W Plug Patterned Wafer Specifications

DATE: May 29, 2007



ATR-35 M1/Via1/M2 Mask Floor Plan
Plug Size: 1100Å - 2500Å
(In order to manufacture SKW5-ATR-35P, we used ATR-35 Via1 mask)



Cross Sectional View

PARAMETER	NOMINAL	TOLERANCE
Patterning		
Center Die X Location	-11.000 mm	+/- 100 µm
Center Die Y Location	-14.500 mm	+/- 100 µm
Die Size: X	22 mm	+/- 10 µm
Die Size: Y	29 mm	+/- 10 µm
Die Stepping (X /Y)	100 / 100 µm	+/- 10%
Wafers must be patterned all the way to the edges of the wafer, i.e. no area anywhere on the wafer unpatterned. (Under certain stepper operating conditions, 2 mm edge edge exclusion is allowed.)		
Line CD Variation (measured on 2 µm structure)		
Lot-to-Lot	2 µm	+/- 10 nm
Within-Lot (Wafer-to-Wafer)		+/- 10 nm
Within-Wafer		+/- 10 nm
Within-Die (measured on 9 trenches)		+/- 10 nm
Pad Oxide thickness		
Lot-to-Lot	10,000 Å	+/- 5 %
Within-Lot (Wafer-to-Wafer)		+/- 5 %
Within-Wafer		+/- 3 %
Within-Die		+/- 3 %
SiN film thickness		
Lot-to-Lot	1000 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
TEOS Oxide film thickness		
Lot-to-Lot	3000 Å	+/- 8 %
Within-Lot (Wafer-to-Wafer)		+/- 8 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %

PARAMETER	NOMINAL	TOLERANCE
PVD TiN film thickness		
Lot-to-Lot	300 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %
CVD W film thickness		
Lot-to-Lot	2500 Å	+/- 10 %
Within-Lot (Wafer-to-Wafer)		+/- 10 %
Within-Wafer		+/- 5 %
Within-Die		+/- 5 %