SKW Cu CMP Patterned Wafers for 90nm Technology Node

Currently, the minimum feature size of most of the Cu/TEOS, Cu/BD, and Cu/BD/SiON CMP patterned wafers commercially available is 0.18µm. These small features can be reliably resolved by using 248nm lithography technology. However, for most of the advanced IC device manufacturing companies, they have been either already deep in the 90nm technology development or are about to move into R&D stage of 65nm technology node. Therefore, we believe our customers should carry out their CMP process development activities using the patterned wafers designed for at least 90nm technology node. This new requirement forces us to design the mask, which contains 0.13µm features. In order to resolve the fine features down to 0.13µm or smaller in size, 193nm lithography technology requires different families of photoresists and new etching technology. The end result of these changes in processing technology is: shallower trench depth (2,000~2500 Å) compared to that of 248nm lithography technology (~5000Å). In order to manufacture the Cu CMP patterned wafers, subsequent barrier layer deposition, Cu seed layer deposition, and Cu electroplating process have to be modified. In order to manufacture the Cu CMP patterned wafers for 90nm technology node, much thinner electroplated Cu layer deposition(4000~5000Å) should be used compared to 10,000-15,000Å currently used for the case of 0.18µm featured sized wafers.

This September we have introduced two different types of Cu CMP patterned wafers for 90nm technology node: 1) SKW 6-3 wafer with 0.13µm minimum feature sizes, and 2) SKW 6-5 wafer with 0.12µm minimum feature sizes. In the case of SKW 6-3 wafer with 0.13µm minimum features sizes, we place one 0.50µm/50µm feature block, from our current 0.18µm SKW 6-3 mask, with 0.13µm/0.13µm feature block. *Figure 1* and *Figure 2* show SKW 6-3 mask with 0.13µm features. Based upon the various integration schemes currently in the semiconductor industry, we have introduced three different types of SKW 6-3 Cu CMP patterned wafers with 0.13µm features in size.

Another type of Cu CMP patterned wafers for 90nm technology node is based upon LSIK194 mask. This reticle has additional features for advanced Cu CMP process characterizations such as interaction length determination, narrow lines with wide dummies, long-range planarization, and others (shown in *Figure 3*). As described above, we have also introduced three different types of SKW 6-5 Cu CMP patterned wafers.

Finally, we also believe our customers will need the multiple-Cu-layer wafers to fully characterize the Cu CMP processes. In order to support these advanced Cu CMP process development activities, we will provide the multiple-Cu-layer wafers (M1/Via1/M2) and/or services to manufacture these kinds of advanced Cu CMP patterned wafers.

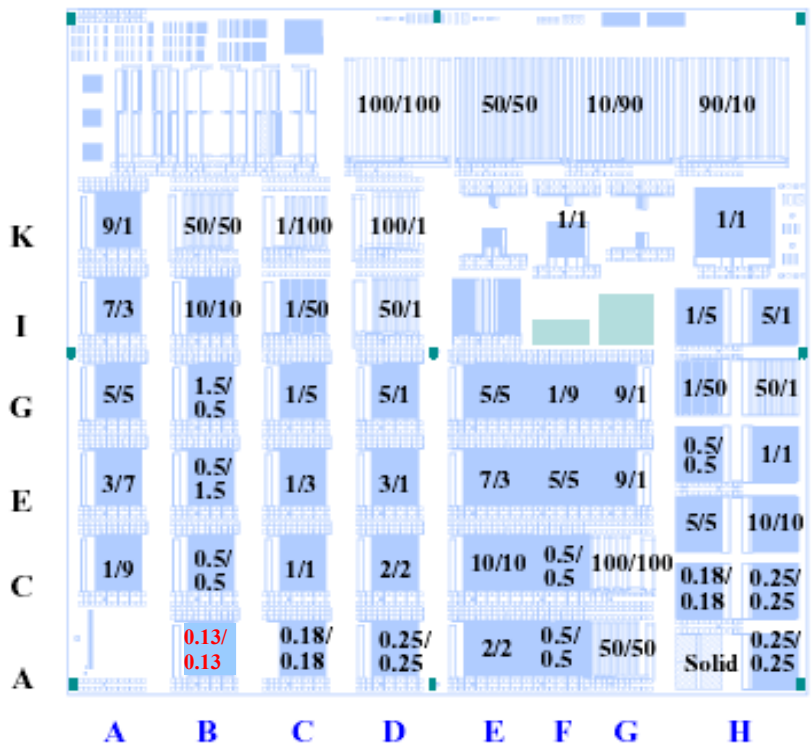

Figure 1
SKW 6-3 Mask
Layout with 0.13µm Features

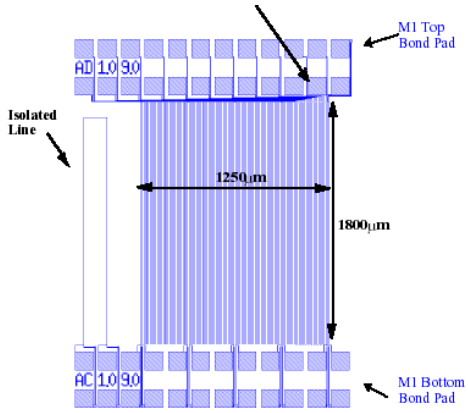

Figure 7 M1 Pattern Structure

Figure 2

SKW 6-3

0.13 μm /0.13 μm feature block

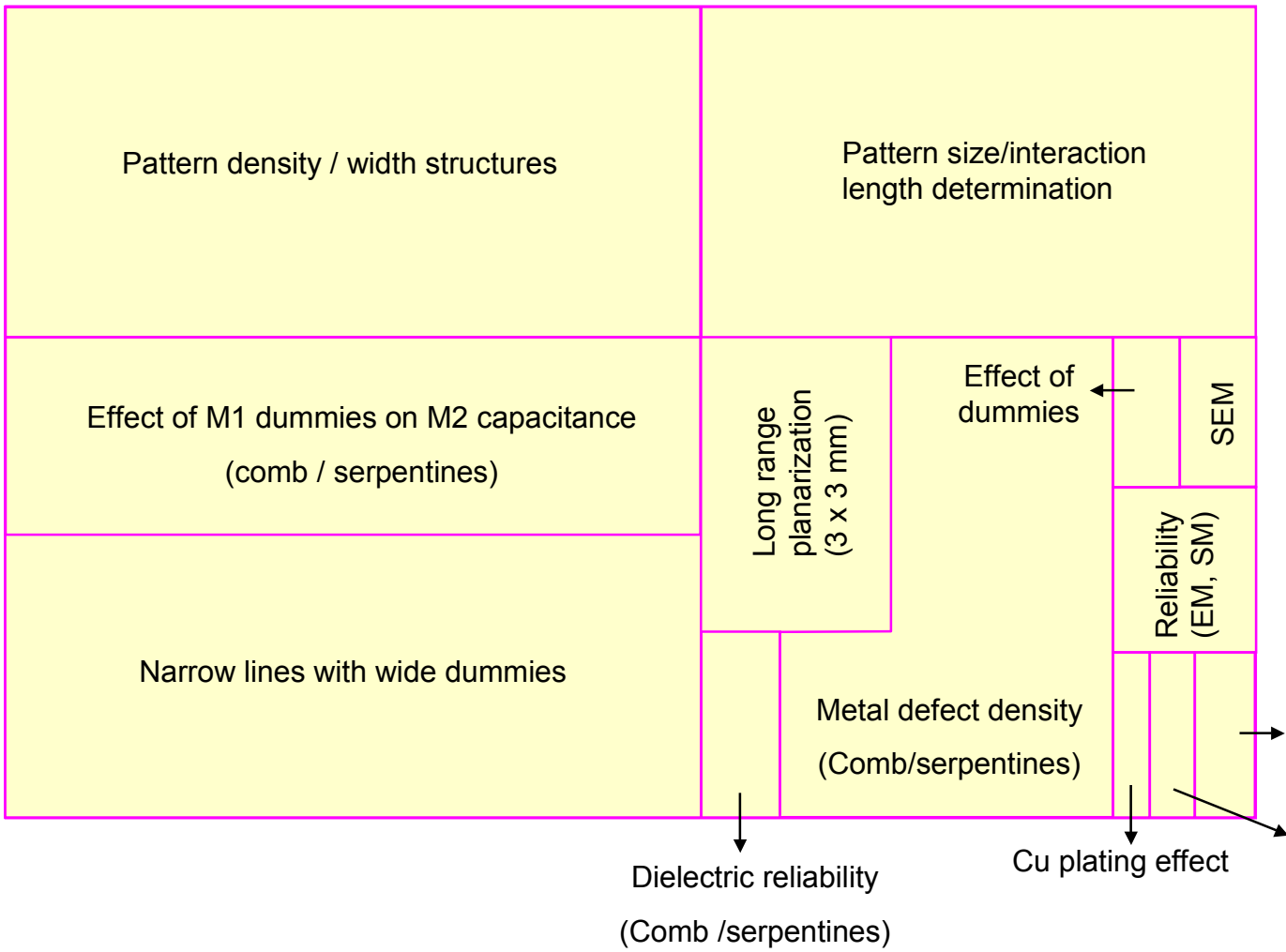

Figure 3

Overall description of LSIK194 mask (this mask is used for manufacturing SKW6-5 wafers for 90nm technology)